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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,901	AMOS ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) *20-52* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Species I claims 1 – 19 in the reply filed on August 18, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Claims 20 – 52 were withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Group II and Species II claims, there being no allowable generic or linking claim. Election was treated as being made **without** traverse in the reply filed on August 18, 2005.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1 – 5, 7 – 9, 12 and 14 – 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karlsson, US 6,867,130 in view of Pey, US 5,153,485.

Regarding claims 1 and 4, Karlsson teaches a process for fabricating a complementary metal oxide semiconductor (CMOS) structure comprising:

- providing a plurality of polySi gates 12 overlying a semiconductor substrate 10 (see Fig. 1);
- forming silicided source/drain regions 17 in the semiconductor substrate (see Fig. 1);
- forming a planarized dielectric stack 30 on the semiconductor substrate (see Fig. 1);
- performing an etching process to expose an upper surface of each polySi gate 12 (see Fig. 3); and
- performing a salicide process which converts each polySi gate to a metal silicide gate 40, wherein each metal silicide gate has substantially the same height, is

composed of the same silicide phase, and has substantially the same work function for the same polySi ion implant conditions (see Fig. 4) in column 1, lines 31 – 42 and in column 4, lines 15 – 62.

Karlsson teaches the first salicidation process of the source/drain regions and the gate in one step without the use of a dielectric cap and therefore fails to teach each polySi gate comprises a dielectric cap located on an upper surface thereof.

Pey teaches a two step salicidation process in which he uses a dielectric cap 20 on the polySi gate 16 with reference to figs 1 and 2 ijn column 4, lines 32 – 62 for the benefit of preventing the exposure of source/drain regions thereby preventing gate to source/drain leakage in column 6, lines 27 – 31.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Karlsson and use a two step salicidation process using a dielectric cap on the polySi gate for the benefit of preventing the exposure of source/drain regions thereby preventing gate to source/drain leakage as taught by Pey in column 6, lines 27 – 31.

Regarding claim 2, Karlsson teaches forming the polySi gates atop a gate dielectric layer 13 with reference to Fig. 1.

Regarding claim 3, Karlsson in view of Pey fails to teach the plurality of polySi gates are formed by deposition, lithography and etching. However, it would have been obvious to one with ordinary skill in the art at the time of the invention form the plurality of polySi gates by deposition, lithography and etching since these are the standard steps for forming gates and are well known in the art.

Regarding claim 5, Karlsson teaches forming one spacer 15 on the gate with reference to Fig. 1.

Regarding claims 7 – 9, 16 and 17, Karlsson teaches the step of forming the silicide contacts on source/drain regions comprises depositing a metal such as Ni atop the semiconductor substrate, and performing a salicide process in column 4, lines 25 – 33.

Regarding claim 12, Karlsson fails to teach the step of forming a planarized dielectric stack comprises deposition and planarization.

Pey teaches a two step salicidation process in which he uses a dielectric stack 28A and planarization with reference to Fig. 2 for the benefit of preventing the exposure of source/drain regions thereby preventing gate to source/drain leakage in column 6, lines 27 – 31.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Karlsson and use a dielectric stack and planarization for the benefit of preventing the exposure of source/drain regions thereby preventing gate to source/drain leakage as taught by Pey in column 6, lines 27 – 31.

Regarding claim 14, Karlsson fails to teach reactive ion etching.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Karlsson and use reactive ion etching since it is a well – known etching process for dielectric layers.

Regarding claims 15, 18 and 19, Karlsson fails to teach the salicide process comprises depositing a blanket silicide metal layer atop the at least the exposed upper

surface of each polySi gate, first annealing to cause total or partial consumption of the polySi gates, selective etching non – reacted silicide metal and optionally performing a second anneal and the respective annealing temperatures.

Pey teaches a two step annealing first at alower temperature and second at a higher temperature to lower the resistivity of the silicide in column 5, lines 14 – 31 for the benefit of preventing the exposure of source/drain regions thereby preventing gate to source/drain leakage in column 6, lines 27 – 31.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Karlsson and use a salicide process comprising depositing a blanket silicide metal layer atop the at least the exposed upper surface of each polySi gate, first annealing to cause total or partial consumption of the polySi gates, selective etching non – reacted silicide metal and optionally performing a second anneal and the respective annealing temperatures for the benefit of preventing the exposure of source/drain regions thereby preventing gate to source/drain leakage as taught by Pey in column 6, lines 27 – 31.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Karlsson, US 6,867,130 in view of Pey, US 5,153,485 as applied to claim 5 above, and further in view of Fu, US 6,596,576.

Karlsson in view of Pey fails to teach at least one spacer includes a first spacer and a second spacer, wherein the first spacer has a thickness that is narrower than the second spacer.

Fu teaches at least one spacer includes a first spacer and a second spacer,

wherein the first spacer has a thickness that is narrower than the second spacer with reference to Fig. 8 for the benefit of preventing the diffusion of hydrogen into the channel in the abstract of the disclosure.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Karlsson in view of Pey and form a first spacer and a second spacer, wherein the first spacer has a thickness that is narrower than the second spacer for the benefit of preventing the diffusion of hydrogen into the channel during the formation of the nitride spacer as taught by Fu in the abstract of the disclosure.

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Karlsson, US 6,867,130 in view of Pey, US 5,153,485 as applied to claim 7 above, and further in view of Kepler, US 6,100,145.

Karlsson in view of Pey fails to teach forming a layer of silicon atop the semiconductor substrate prior to metal deposition.

Kepler teaches forming a layer of silicon atop the semiconductor substrate prior to metal deposition for the benefit of lowering the consumption of the silicon from the substrate in the abstract of the disclosure.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Karlsson in view of Pey and form a layer of silicon atop the semiconductor substrate prior to metal deposition for the benefit of lowering the consumption of the silicon from the substrate as taught by Kepler in the abstract of the disclosure.

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Karlsson, US 6,867,130 in view of Pey, US 5,153,485 as applied to claim 1 above, and further in view of Cave, US 6,924,184.

Karlsson in view of Pey fails to teach the step of forming a planarized dielectric stack comprising forming an etch stop layer, forming an interlevel dielectric and planarizing the interlevel dielectric.

Cave teaches the step of forming a planarized dielectric stack comprising forming an etch stop layer, forming an interlevel dielectric and planarizing the interlevel dielectric with reference to Fig. 8 for the benefit of establishing a top surface that is very uniform in height above the substrate across the wafer in the abstract of the disclosure.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Karlsson in view of Pey and forming a planarized dielectric stack comprising forming an etch stop layer, form an interlevel dielectric and planarizing the interlevel dielectric for the benefit of establishing a top surface that is very uniform in height above the substrate across the wafer as taught by Cave in the abstract of the disclosure.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok Kumar Sarkar
Asok K. Sarkar
September 6, 2005

Primary Examiner